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EXAMINER	
PEREZ DAPLE, AARON C	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/816,752	SUZUOKI ET AL.	
	Examiner	Art Unit	
	Aaron C Perez-Daple	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *see note attached*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

NOTE: IDS forms attached, 6/1/04, 3/11/04, 3/3/03, 9/4/02, 9/10/01.

DETAILED ACTION

1. This Action is in response to Application filed 3/22/01.

2. Claims 1-38 are presented for examination.

3. This Action is non-Final.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1-5, 15, 20-22, 35-38** are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US 5,581,777 B1) (hereinafter Kim).

6. As for claims 1 and 20, Kim discloses a computer processor comprising:

a main memory for storing programs and data associated with said programs (cluster memory 54, Fig. 2);

a plurality of first processing units (processors 49, Fig. 2) for processing said programs and said associated data, each said first processing unit including a local memory exclusively associated with said first processing unit (stage registers 52, Fig. 2);

a second processing unit (ACU 20, Fig. 2) for controlling said processing of said programs and said associated data by said first processing units, said second processing unit being operable to direct any one of said first processing units to process one of said programs by directing the transfer of said one program and data associated with said one program from said main memory to the local memory exclusively associated with said one first processing unit and instructing said one first processing unit to initiate processing of said one program, said one first processing unit thereafter processing said one program and said data associated with said one program from said local memory exclusively associated with said one first processing unit (col. 5, lines 42-63).

7. As for claim 2, Kim discloses the processor of claim 1, wherein said main memory is a dynamic random access memory (col. 9, lines 23-35).

8. As for claim 3, Kim discloses the processor of claim 1, wherein said main memory includes a plurality of memory locations, each said memory location including a memory segment exclusively associated with said memory location (col. 12, line 66 – col. 13, line 17).

9. As for claim 4, Kim discloses the processor of claim 3, wherein each said memory segment stores status information indicating the status of data stored in said memory segment's associated memory location, the identity of a first processing unit and a memory address (col. 9, lines 29-35).

10. As for claim 5, Kim discloses the processor of claim 4, wherein said status information indicates the validity of said data stored in said memory segment's associated memory location (col. 9, lines 29-35), said identity indicates the identity of a particular one of said

first processing units and said memory address indicates a storage location within the local memory exclusively associated with said particular one first processing unit (col. 12, line 43 – col. 13, line 17).

11. As for claim 15, Kim discloses the processor of claim 1, further comprising means for prohibiting each said first processing unit from reading data from, or writing data to, any of said local memories with which said first processing unit is not exclusively associated (col. 6, lines 11-50).

12. As for claims 21 and 22, Kim teaches configuring a processing element with various numbers of processing units, including 4 and 8 processing units (col. 4, line 65 – col. 5, line 30; Fig. 2).

13. As for claims 35-38, Kim teaches varying the number of processor modules, including 1, 2, 4 and 8 processor modules (col. 4, line 65 – col. 5, line 30; Fig. 2).

14. **Claims 1-3 and 20** are further rejected and **claims 16-19** are rejected under 35 U.S.C. 102(e) as being anticipated by Hofstee et al. (US 2002/0078285 A1) (hereinafter Hofstee).

The applied reference has a common assignee and at least one common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

15. As for claims 1 and 20, Alvarez discloses a computer processor comprising:

a main memory for storing programs and data associated with said programs (shared memory 10, Fig. 1);

a plurality of first processing units (APU 230A-T, Fig. 2) for processing said programs and said associated data, each said first processing unit including a local memory exclusively associated with said first processing unit (local memory is inherent for copying data to/from the APU as described in paragraph 0028);

a second processing unit (PU 210A-D, Fig. 2) for controlling said processing of said programs and said associated data by said first processing units, said second processing unit being operable to direct any one of said first processing units to process one of said programs by directing the transfer of said one program and data associated with said one program from said main memory to the local memory exclusively associated with said one first processing unit and instructing said one first processing unit to initiate processing of said one program, said one first processing unit thereafter processing said one program and said data associated with said one program from said local memory exclusively associated with said one first processing unit (paragraph 0028).

16. As for claim 2, Hofstee discloses the processor of claim 1, wherein said main memory is a dynamic random access memory (paragraph 0023).

17. As for claim 3, Hofstee discloses the processor of claim 1, wherein said main memory includes a plurality of memory locations, each said memory location including a memory segment exclusively associated with said memory location (memory is inherently segmented according to address locations in order for systems to access the data).

18. As for claim 16, Hofstee discloses the processor of claim 1, further comprising a direct memory access controller (DMA 220A-D, Fig. 2).

19. As for claim 17, Hofstee discloses the processor of claim 16, wherein said second processing unit directs said transfer of said one program and said data associated with said one program to the local memory exclusively associated with said one first processing unit by issuing a command to said direct memory access controller and, in response to said command, said direct memory access controller transfers said one program to the local memory exclusively associated with said one first processing unit (paragraph 0028).

20. As for claim 18, Hofstee discloses the processor of claim 17, wherein said one first processing unit directs the transfer of further data for processing said one program from said main memory to the local memory exclusively associated with said one first processing unit by issuing a command to said direct memory access controller and, in response to said command, said direct memory access controller transfers said further data to the local memory exclusively associated with said one first processing unit (paragraphs 0012, 0040).

21. As for claim 19, Hofstee discloses the processor of claim 18, wherein said one first processing unit directs a transfer of data resulting from said processing of said one program from the local memory exclusively associated with said one first processing unit to said main memory by issuing a command to said direct memory access controller and, in response to said command, said direct memory access controller transfers said resulting data from the local memory exclusively associated with said one processing unit to said main memory (paragraphs 0012, 0040).

22. **Claims 1-3 and 16-20** are further rejected and claims **6-8, 10-13, 23-28 and 30** are rejected under 35 U.S.C. 102(b) as being anticipated by Guttag et al. (US 5,487,146) (hereinafter Guttag).

23. As for claims 1 and 20, Guttag discloses a computer processor comprising:

a main memory for storing programs and data associated with said programs (memory 9, Fig. 1; col. 9, lines 12-25);

a plurality of first processing units (processors 60, 71-74, Fig. 2) for processing said programs and said associated data, each said first processing unit including a local memory (memory 20) exclusively associated with said first processing unit (col. 10, lines 21-47);

a second processing unit (transfer controller 80, Fig. 2) for controlling said processing of said programs and said associated data by said first processing units, said second processing unit being operable to direct any one of said first processing units to process one of said programs by directing the transfer of said one program and data associated with said one program from said main memory to the local memory exclusively associated with said one first processing unit and instructing said one first processing unit to initiate processing of said one program, said one first processing unit thereafter processing said one program and said data associated with said one program from said local memory exclusively associated with said one first processing unit (col. 12, lines 35-57).

24. As for claim 2, Guttag discloses the processor of claim 1, wherein said main memory is a dynamic random access memory (col. 12, lines 54-57).

25. As for claim 3, Guttag discloses the processor of claim 1, wherein said main memory includes a plurality of memory locations, each said memory location including a memory

segment exclusively associated with said memory location (memory is inherently segmented according to address locations in order for systems to access the data).

26. As for claim 6, Guttag discloses the processor of claim 1, wherein each of said first processing units is a single instruction multiple data processor (col. 12, lines 23-25).

27. As for claim 7, Guttag discloses the processor of claim 1, wherein each of said first processing units includes a set of registers, a plurality of floating points units, and one or more buses connecting said set of registers to said plurality of floating point units (col. 11, lines 40-55).

28. As for claim 8, Guttag discloses the processor of claim 7, wherein each of said first processing units further includes a plurality of integer units and one or more buses connecting said plurality of integer units to said set of registers (col. 11, lines 40-55).

29. As for claim 10, Guttag discloses the processor of claim 1, wherein said local memories are static random access memories (col. 10, lines 27-29).

30. As for claim 11, Guttag discloses the processor of claim 1, further comprising a rendering engine for generating pixel data, a frame buffer for temporarily storing said pixel data and a display controller for converting said pixel data to a video signal (col. 12, line 58 – col. 13, line 5).

31. As for claim 12, Guttag discloses the processor of claim 1, wherein the data associated with said one program includes a stack frame (col. 12, line 58 – col. 13, line 5).

32. As for claim 13, Guttag discloses the processor of claim 1, wherein each said first processing unit comprises a controller for directing, during said processing of said programs

and said associated data, a transfer of further data from said main memory to the local memory exclusively associated with said first processing unit (col. 12, lines 35-57).

33. As for claim 16, Guttag discloses the processor of claim 1, further comprising a direct memory access controller (col. 12, lines 35-37).

34. As for claim 17, Guttag discloses the processor of claim 16, wherein said second processing unit directs said transfer of said one program and said data associated with said one program to the local memory exclusively associated with said one first processing unit by issuing a command to said direct memory access controller and, in response to said command, said direct memory access controller transfers said one program to the local memory exclusively associated with said one first processing unit (col. 12, lines 35-57).

35. As for claim 18, Guttag discloses the processor of claim 17, wherein said one first processing unit directs the transfer of further data for processing said one program from said main memory to the local memory exclusively associated with said one first processing unit by issuing a command to said direct memory access controller and, in response to said command, said direct memory access controller transfers said further data to the local memory exclusively associated with said one first processing unit (col. 12, lines 35-57).

36. As for claim 19, Guttag discloses the processor of claim 18, wherein said one first processing unit directs a transfer of data resulting from said processing of said one program from the local memory exclusively associated with said one first processing unit to said main memory by issuing a command to said direct memory access controller and, in response to said command, said direct memory access controller transfers said resulting data from the

local memory exclusively associated with said one processing unit to said main memory (col. 12, lines 35-57).

37. As for claim 23, Guttag discloses the processing apparatus of claim 20, wherein each of said processor modules comprises only one second processing unit (transfer controller 80, Fig. 2).

38. As for claim 24, Guttag discloses the processing apparatus of claim 20, wherein each of said processor modules further comprises a direct memory access controller, said direct memory access controller being responsive to commands from said first processing units and said second processing unit to effect transfers of said programs and said associated data between said main memory and said local memories (col. 12, lines 35-57).

39. As for claim 25, Guttag discloses the processing apparatus of claim 20, wherein each of said processor modules further comprises a local bus for providing communications among said first processing units and said second processing unit (col. 10, lines 6-20; Fig. 2).

40. As for claim 26, Guttag discloses the processing apparatus of claim 20, further comprising a module bus for providing communications among said processor modules (col. 10, lines 6-20; Fig. 2).

41. As for claim 27, Guttag discloses the processing apparatus of claim 20, further comprising a memory bus for providing communications between each of said processor modules and said main memory (image system bus, Fig. 1; col. 8, lines 43-45).

42. As for claim 28, Guttag discloses the processing apparatus of claim 20, wherein each of said first processing units comprises a plurality of floating point units and a plurality of integer units (col. 11, lines 40-55).

43. As for claim 30, Guttag discloses the processing apparatus of claim 20, wherein at least one of said processor modules further comprises a rendering engine for generating pixel data, a frame buffer for temporarily storing said pixel data and a display controller for converting said pixel data to a video signal (col. 12, line 58 – col. 13, line 5).

Claim Rejections - 35 USC § 103

44. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

45. **Claims 14 and 31-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Guttag in view of Alvarez et al (US 6,467,012 B1) (hereinafter Alvarez).

46. As for claims 14 and 31-34, although Guttag teaches the use of a crossbar (cross-bar 50, Fig. 2), Guttag does not explicitly disclose a crossbar for connecting a plurality of memory bank controllers to each of said first processing units. Alvarez discloses a crossbar for connecting a plurality of memory bank controllers to each of a plurality of processing units (address switch 430, Fig. 4; col. 8, lines 40-47; Fig. 5; col. 9, lines 22-36). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Guttag by using a crossbar for connecting a plurality of memory bank controllers to each of said first processing units in order to increase the memory capacity and speed of the system, as taught by Alvarez above.

47. **Claims 15** is further rejected under 35 U.S.C. 103(a) as being unpatentable over Guttag in view of Chi et al (US 5,940,870) (hereinafter Chi).

48. As for claim 15, Guttag does not specifically disclose prohibiting each first processing unit from writing data to or reading data from any of the local memories with which the first processing unit is not exclusively associated. Chi teaches prohibiting each first processing unit from writing data to or reading data from any of the local memories with which the first processing unit is not exclusively associated (col. 2, lines 53-57; col. 3, lines 18-29). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Guttag by prohibiting each first processing unit from writing data to or reading data from any of the local memories with which the first processing unit is not exclusively associated in order to increase the efficiency of memory utilization, as taught by Chi (col. 3, lines 9-15).

49. **Claims 9 and 29** are rejected under 35 U.S.C. 103(a) as being obvious over Guttag in view of Chin et al. (US 5,497,465) (hereinafter Chin).

50. As for claims 9 and 29, Guttag does not specifically disclose an optical interface and an optical waveguide for converting electrical signals generated by said processor to optical signals for transmission from said processor and to convert optical signals transmitted to said processor to electrical signals, said optical waveguide being connected to said optical interface for transmitting said optical signals. Chin discloses an optical interface and an optical waveguide for converting electrical signals generated by said processor to optical signals for transmission from said processor and to convert optical signals transmitted to said processor to electrical signals, said optical waveguide being connected to said optical

interface for transmitting said optical signals (col. 6, line 51 – col. 7, line 19). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Guttag by using an optical interface and an optical waveguide for converting electrical signals generated by said processor to optical signals for transmission from said processor and to convert optical signals transmitted to said processor to electrical signals for the purpose of reducing the number of electrical connections and increasing the speed of data transferred (col. 7, lines 13-19).

51. **Claims 4, 5, 21, 22, and 35-38** are further rejected under 35 U.S.C. 103(a) as being obvious over Guttag in view of Kim et al. (US 5,581,777) (hereinafter Kim).

52. As for claims 4 and 5, Guttag does not specifically disclose storing status information indicating the validity of the data stored and an identity indicating the identity of a particular one of the first processing units. Kim discloses the processor of claim 4, wherein said status information indicates the validity of said data stored in said memory segment's associated memory location (col. 9, lines 29-35), said identity indicates the identity of a particular one of said first processing units and said memory address indicates a storage location within the local memory exclusively associated with said particular one first processing unit (col. 12, line 43 – col. 13, line 17). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Guttag by storing status information indicating the validity of the data stored and an identity indicating the identity of a particular one of the first processing units in order to efficiently access stored data, as taught by Kim (col. 9, lines 29-35).

53. As for claims 21 and 22, Guttag does not specifically disclose varying the number of processing units. Kim teaches configuring a processing element with various numbers of processing units in order to optimize the system for a specific application (col. 4, line 65 – col. 5, line 17). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Guttag by varying the number of processing units in order to optimize the system for a specific application, as taught by Kim above.

54. As for claims 35-38, Guttag does not specifically disclose varying the number of processor modules. Kim teaches varying the number of processor modules in order to optimize the system for a specific application (col. 4, line 65 – col. 5, line 30; Fig. 2). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Guttag by varying the number of processor modules in order to optimize the system for a specific application, as taught by Kim above.

Conclusion

55. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

US 5,131,054, note Fig. 1;

US 5,093,879, note teaches optical connections for processor system;

US 5,037,173, note teaches optical crossbar switch;

US 5,056,000, note abstract;

US 6,173,389 B1, note Fig. 3;

US 6,209,065 B1, note Fig. 1;

US 6,647,208 B1, note teaches hybrid electro-optical system.

56. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron C Perez-Daple whose telephone number is (571) 272-3974. The examiner can normally be reached on 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Follansbee can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/6/04

Aaron Perez-Daple